MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Crystal Oscillator Circuit Design

In this application note we shall discuss our recommended crystal oscillator circuit, explain each component in the circuit and provide some guidelines on selecting values for these components. Finally, we shall give a few precautions to take in order to avoid in-stability and start-up problems.

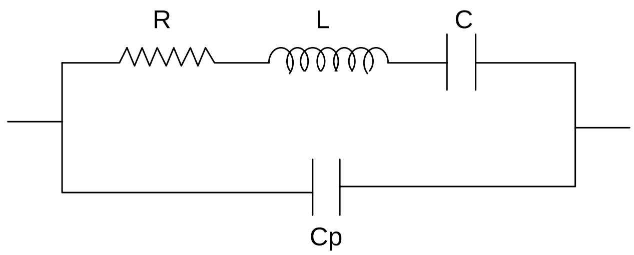

Figure 1. Crystal equivalent Circuit.

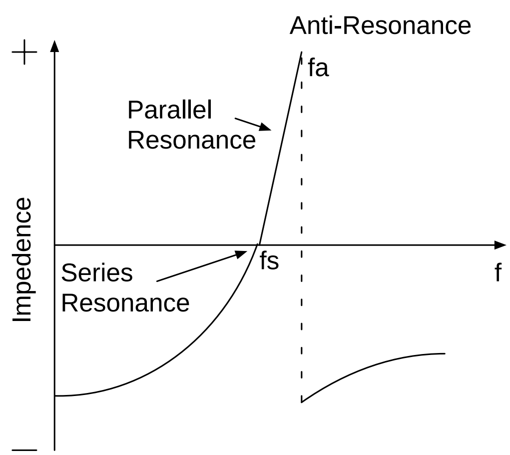

Figure 2. Reactance Vs Frequency plot of a crystal.

Figure 1. shows the crystal equivalent circuit. R is the effective series resistance, L and C are the motional inductance and capacitance of the crystal. C_P is the shunt capacitance due to the crystal electrodes. Figure 2. shows the reactance-frequency plot of the crystal. When a crystal is operating at series resonance it looks purely resistive and the reactances of the inductor and the capacitor are equal (XL = XC). The series resonance frequency is given by the equation

$$fs = \frac{1}{2\pi\sqrt{LC}}$$

When the crystal is operating in parallel resonant mode it looks inductive. The frequency of operation in this mode is defined by the load on the crystal. The crystal manufacturer should specify the load capacitance C_L for parallel resonant crystals. In this mode the frequency of oscillation is given by the equation.

$$f_a = \frac{1}{2\pi\sqrt{L\frac{C_L C_P}{C_L + C_P}}}$$

In parallel resonance mode the crystal can be made to oscillate anywhere on the f_s - f_a slope of the reactance plot, shown in Figure 2, by varying the load of the crystal. All of MX-COM's crystal oscillator circuits recommend using parallel resonant mode crystals.

Figure 3. shows the recommended Crystal oscillator circuit diagram. In this type of setup the crystal is expected to oscillate in parallel resonant mode. The inverter which is internal to the chip acts as class AB amplifier and provides approximately 180° phase shift from input to the output and the π network formed by the crystal, R_1, C_1 and C_2 provides additional 180° phase shift. So the total phase shift around the loop is 360°. This satisfies one of the conditions required to sustain oscillation. The other condition, for proper startup and sustaining oscillation is the closed loop gain should be ≥ 1.

The resistor R_f around the inverter provides negative feedback and sets the bias point of the inverter near mid-supply operating the inverter in the high gain linear region. The value of this resistor is high, usually in the range of a 500KΩ ~ 2MΩ. Some of MXCOM's ICs have this resistor internal, refer to the external component specifications in the data sheet of a particular chip.

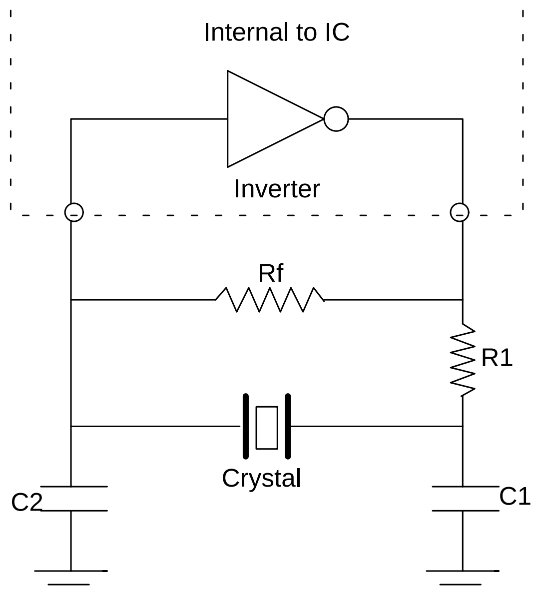

Figure 3. Crystal oscillator circuit.

The capacitors C_1 and C_2 form the load capacitance for the crystal. The optimum load capacitance (C_L) for a given crystal is specified by the crystal manufacturer. The equation to calculate the values of C1 and C2 is

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_S$$

Where C_S is the stray capacitance on the printed circuit board, typically a value of 5pf can be used for calculation purposes. Now C_1 and C_2 can be selected to satisfy the above equation. Usually C_1 and C_2 are selected such that they are approximately equal. Large values of C_1 and/or C_2 increases frequency stability but decreases loop gain and may cause start-up problems.

R_1 is the drive limiting resistor, the primary function of this resistor is to limit the output of the inverter so that the crystal is not over driven. R_1 and C_1 form a voltage dividing circuit, the values of these components are chosen in such a way that the output of the inverter goes close to rail-to-rail and the input to the crystal is 60% of rail-to-rail, usual practice is to make resistance of R_1 and reactance of C_1 equal at the operating frequency, i.e. $R_1 \approx XC_1$. This makes the input to the crystal half that of the inverter output. Always make sure that the power dissipated by the crystal is with-in the crystal manufacturer's specifications. Over-driving the crystal may damage the crystal. Please refer to the crystal manufacturer's recommendations.

Ideally the inverter provides 180° phase shift, but the inherent delay of the inverter provides additional phase shift proportional to the delay. In order to ensure the total phase shift of *n*360° around the loop, the π network should provide 180° less the phase shift due to the inverter delay. R1 can be varied to accomplish this. With fixed C_1 and C_2, the closed loop gain and phase can be altered by varying R_1. In some applications R_1 can be ignored if the above two conditions are met.

Some ICs have all the external components (R_f, R_1, C_1, and C_2) internal to the chip, thus eliminating worries to the circuit designer. In this case simply connect the crystal across the XTAL and XTAL pins.

Hints:

Select a crystal with low effective series resistance (ESR), which helps with crystal start-up problems. Lower ESR increases the loop gain.

Reduce the stray capacitance on the board layout by shortening the traces. This would help with startup problem and as well as the frequency of oscillation.

Always test the circuit in applicable temperature and voltage ranges to ensure the crystal starts and sustains oscillations and tweak the component values if necessary.

For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of Vdd, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain further crystal oscillator design assistance, consult your crystal manufacturer.

The recommended way to optimize R_1 is first calculate C_1 and C_2 as explained earlier and connect a potentiometer in place of R_1, set its initial setting at approximately equal to XC_1, then vary the potentiometer setting if required until the crystal starts under all conditions and sustains oscillation under steady state condition.